forming interconnection structures of conductor material on a face of a second wafer of semiconductor material, including forming plug elements each having a bonding region of a metal material capable of reacting with said semiconductor material of said first wafer;

forming self-alignment structures on the respective faces of said first and second wafers, and aligning said first and second wafers in a face-to-face configuration, using said self-alignment structures and

bonding said first wafer and said second wafer together, including causing said bonding regions to react with said semiconductor material of said first wafer.

Cont B5

37. (New) A process for manufacturing an integrated device, comprising:

forming a structure in a first wafer of semiconductor material, including a movable component;

forming an integrated electronic component in a second wafer of semiconductor material;

forming a bonding layer, including a base region and a bonding region of a metal material on a selected one of the first or second wafer; and

bonding the first and second wafers together by causing the bonding region of the bonding layer to react with an exposed semiconductor material region on the one of the first or second wafers not selected.

REMARKS

Claims 1-12 and 30-37 will be pending upon entry of the present amendment. Claims 1, 4, 5, 11, and 30 have been amended. New claims 31 through 37 are herein submitted. Claims 13-29 are cancelled.

Applicant thanks the Examiner for indicating allowability of the subject matter of claims 4 and 10-12.

The Examiner has objected to claims 4 and 5 because of informalities therein. Amendments to claims 4 and 5 include corrections to those informalities.

The Examiner has rejected claims 5 and 8 under 35 U.S.C. § 112, first paragraph, stating that the inventor is not allowed to claim the combination of two different figures into a single group of claims. Applicant is unable to understand the basis of this rejection. The rejected claims 5 and 8 are dependent claims of the independent claim 1, which reads on Figures 10-12. For example, with reference to the device of Figure 10, the device includes semiconductor regions 58, 59 and isolation regions 55 of the first wafer of semiconductor material 51. The device further includes interconnection structures including plug elements comprising base regions 69 and bonding regions 70 of the second wafer of semiconductor material 52. Finally, the device shows the first and second wafers bonded together by the interconnection structures. Thus, claim 1 reads on the Figure 10, and in a similar way on Figures 11 and 12. Applicant is unaware of any rule or statue which requires that all of the dependent claims of an independent claim be limited to a common set of figures, and requests that, in the even that the Examiner is aware of such a rule, that the Examiner provide that reference to the applicant.

The Examiner has rejected claim 30 under 35 U.S.C. § 102(b) as being anticipated by Temple et al. (PN 5,654,226), and claims 1-3, 6-7, and 9 under 35 U.S.C. § 103(a) as being unpatentable over Temple in view of Yu et al. (PN 5,801,083).

Claim 1 has been amended to make more explicit the structure of the plug elements recited therein. Claim 1 now recites in part "forming interconnection structures . . . including forming plug elements, each *including a base region and* a bonding region, *the bonding region* of a metal material capable of reacting with said semiconductor regions of said first wafer." In rejecting claim 6, which also recites the structure of the plug elements including a base region and a conductive material, the Examiner has cited a lower portion of the silicide bond 18 of Temple as being the equivalent of the base region and an upper portion of the same silicide bond 18 as being the equivalent of the bonding regions of claim 6. Temple fails to differentiate between an upper and lower portion of the silicide bond, and fails to teach any benefit or reason to form a plug element including the separate base and bonding regions (column 2, line 67; column 3, lines 45-50; and column 4, lines 30-32). In contrast, amended claim 1 specifically recites plug elements each including the base region and a bonding region of a metal material different from the base region. Support for this amendment may be found, for

example, on page 5 of the specification, lines 10-13, and page 9, lines 18-20. Accordingly, claim 1 is now allowable over Temple in view of Yu. Dependent claims 2-12 and 31-33 are also now allowable over Temple in view of Yu.

Claim 9 is allowable on its own merits, apart from its dependence upon an allowable independent claim, inasmuch as conventional alignment methods require the optical alignment of targets or optical references provided on visible surfaces of substrates to be aligned, and bonding the substrates while maintaining the alignment of the references. In contrast, self-alignment structures on wafers to be aligned, as recited in claim 9, provide secure alignment through physical contact as opposed to previous methods, which, because they require the external monitoring of references to maintain correct positioning, can't be regarded as "self-aligning." Accordingly, claim 9 is allowable.

Dependent claim 31 is also allowable on its merit. Claim 31 recites palladium as the metal material. Temple teaches the use of titanium, molybdenum, tungsten, or platinum as appropriate metals for formation of the silicide bond 18, further noting that the bond is formed at about 700°C. In contrast, the use of palladium is particularly advantageous, inasmuch as it allows bonding at low temperature (less than 400°C), thus allowing the bonding of the first and second wafers at a late manufacturing stage without risking damage to diffused regions and other components already formed therein. This advantage is not taught by Temple, and is therefore patentable thereover. Support for new claim 31 may be found on page 5, line 12 and line 27.

New claim 32 recites forming a through opening in a second wafer on a side of the wafer opposite the interconnection structures, such that a portion of an interconnection structure is exposed. New claim 33 recites further attaching a connection wire to the interconnection structure via the through opening. Support for claims 32 and 33 may be found in the specification on page 10, lines 20-24, and Figure 10.

New claim 34 includes the limitations of the allowable claim 4.

The complete text of new claim 35 is shown herebelow:

35. (New) A process for manufacturing an integrated device, comprising:

forming integrated structures including semiconductor regions and isolation regions in a first wafer of semiconductor material;

forming interconnection structures of conductor material on a second wafer of semiconductor material, including forming plug elements, each having a bonding region of a metal material capable of reacting with said semiconductor regions of said first wafer;

forming a plurality of conductive regions on the second wafer;

forming connection regions connecting the conductive regions together;

forming at least one of the plug elements connected to one of the plurality of conductive regions; and

bonding said first wafer and said second wafer together, including causing said bonding regions to react with said semiconductor regions.

The above limitations of new claim 35 are not anticipated or made obvious by the cited prior art. Temple et al. discloses a process for fabricating discreet components, that is, after dicing only a single component is comprised in each chip. Thus, Temple fails to teach forming a plurality of conductive regions on the second wafer, forming connection regions connecting the conductive regions together, and further fails to teach forming at least one of the plug elements connected to one of the plurality of conductive regions. Accordingly, new claim 35 is allowable over the cited prior art.

New claim 36 recites in part, "forming self-alignment structures on the respective faces of said first and second wafers, and aligning said first and second wafers in a fact-to-face configuration, using said self-alignment structures." Temple fails to teach any alignment structures on the wafers. Conventional alignment methods rely on visible alignment structures, meaning that structures on wafers to be bonded must be on visible surfaces of the wafers. In contrast, claim 36 recites alignment structures on wafers on a face-to-face configuration, meaning that the alignment structures of one or the other of the wafers would be invisible when correctly aligned. Accordingly, claim 36 is allowable over the cited prior art.

New claim 37 recites, in part, "forming a structure in a first wafer of semiconductor material, including a movable component; forming an integrated electronic component in a second wafer of semiconductor material; and bonding the first and second wafers together." Temple fails to teach the formation of any structures with movable components, and therefore fails to anticipate the limitations of claim 37, which is therefore allowable.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited. In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicant's undersigned representative at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Commissioner is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment to our Deposit Account No. 19-1090.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version With Markings to Show Changes Made.**"

Respectfully submitted,

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HHB:wt

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 1, 4, 5, 11, and 30 have been amended.

Claims 31-37 are new.

1. (Amended) A process for manufacturing an integrated device, comprising:

forming integrated structures including semiconductor regions and isolation regions in a first wafer of semiconductor material;

forming interconnection structures of conductor material on a second wafer of semiconductor material, including forming plug elements, each including a base region and ~~having~~ a bonding region, the bonding region of a metal material different from the base region and capable of reacting with said semiconductor regions of said first wafer; and

bonding said first wafer and said second wafer together, including causing said bonding regions to react with said semiconductor regions.

4. (Amended) The process according to claim 1, wherein said plug elements have a height, and said step of forming integrated structures comprises forming an insulating material layer on top of ~~a substrate of semiconductor material~~the first wafer, said insulating material layer having a thickness smaller than said height of said plug elements, and forming openings in said insulating material layer to uncover selective portions of said ~~substrate~~wafer ~~(2)~~, and wherein said step of bonding said first and second wafers comprises causing said bonding region to react with at least said selective portions of said ~~substrate~~wafer.

5. (Amended) The process according to claim 1, wherein said step of forming integrated structures comprises forming an insulating material layer on top of ~~a substrate of semiconductor material~~the first wafer, and forming conductive regions ~~(~~of semiconductor

material on top of said insulating material layer, and said step of bonding said first and second wafers comprises causing said bonding region to react with said conductive regions.

11. (Amended) The process according to claim 10, wherein said step of forming integrated structures comprises forming an insulating material layer on top of ~~a substrate of semiconductor material~~the first wafer, said step of forming at least one engagement seat comprises forming a guide opening in said insulating material layer, said guide opening having a basically trapezium shape, with a major base and a minor base, and said engagement element having transverse dimensions smaller than said major base and greater than said minor base, and said step of aligning said first and second wafers comprises inserting said engagement element into said guide opening near said major base and displacing said second wafer with respect to said first wafer so to bring said engagement element towards said guide opening until said engagement element slots into said engagement seat.

30. (Amended) A process for manufacturing an integrated device, comprising:

forming integrated structures in a first wafer of semiconductor material, the first wafer including an exposed semiconductor region;

forming a ~~bonding layer~~plug element, including a base region and a bonding region, the bonding region of a metal material on a second wafer of semiconductor material; and

bonding the first and second wafers together by causing the bonding region of the ~~bonding layer~~plug element to react with the exposed semiconductor region.